REMARKS

Regarding the Final Office Action:

In the Final Office Action, the Examiner:

> rejected claims 1-5, 11-14, and 20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,396,772 to Yabe et al. ("*Yabe*");
>
> rejected claims 1, 2, 12, 13, and 20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,785,435 to Inoue ("*Inoue*"); and
>
> objected to claims 6-10 and 14-19 as being dependent from a rejected claim, but allowable if rewritten in independent form.

Applicant amends claims 1, 5-10, and 14-19, and cancels claim 2. Thus, claims 1 and 3-20 remain pending and under current examination.

Applicant respectfully traverses the rejections and objections, for the following reasons[1].

Rejection of Claims under 35 U.S.C. §102:

In order to properly establish anticipation under 35 U.S.C. § 102, the Federal Circuit has held that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim."

[1] The Final Office Action may contain statements characterizing the related art, case law, and claims. Regardless of whether any such statements are specifically identified herein, Applicant declines to automatically subscribe to any statements in the Final Office Action.

Richardson v. Suzuki Motor Co., 868 F.2d 1126, 1236 (Fed. Cir. 1989). *See also* M.P.E.P. § 2131.

Rejection of Claims 1-5, 11-14, and 20 under 35 U.S.C. § 102(e) as being anticipated by *Yabe*:

Applicant traverses the rejection of claims 1-5, 11-14 and 20 under 35 U.S.C. § 102(e) as being anticipated by *Yabe*.

Yabe does not disclose each and every element of the amended claims. For example, *Yabe* does not disclose at least a "a control circuit for, in response to the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit, controlling the switch circuit to turn on in order to connect the first power source and the second power source so that the first power source is charged by the second power source, thereby operating the clock circuit," as recited in amended claim 1.

The Office asserts that the central control circuit 93 of *Yabe* corresponds to the claimed "control circuit," the step-up/down circuit 49 of *Yabe* corresponds to the claimed "switch circuit," and the voltage detecting circuit 92 of *Yabe* corresponds to the claimed "power source input detecting circuit" (FOA at 2). However, *Yabe* merely teaches that "voltage detecting circuit 92" is "for detecting a charging voltage VC of the large-capacity secondary power supply 48 and an output voltage of the step-up/down circuit 49." (*Yabe* at col. 14, ll. 14-16.) That is, *Yabe* is silent with respect to "the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit," as recited in claim 1.

The Office appears to contend that because the voltage detecting circuit 92 of *Yabe* "detect the input of the second power source at all times" (FOA at 6), *Yabe* necessarily discloses "detecting the insertion of the second power source during a halted state of the clock circuit," as amended in claim 1. However, even if such a contention were correct, which Applicant does not concede, *Yabe* still fails to teach or suggest that its central control circuit 93 controls its step-up/down circuit 49 "in response to the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit," as recited in claim 1. Therefore, *Yabe* cannot teach or suggest "a control circuit for, in response to the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit, controlling the switch circuit to turn on in order to connect the first power source and the second power source so that the first power source is charged by the second power source, thereby operating the clock circuit," as recited in amended claim 1.

For at least these reasons, *Yabe* does not disclose each and every element recited in claim 1 as is required to uphold a rejection under 35 U.S.C. § 102(e). *Yabe* thus does not anticipate claim 1. Claims 2-5, 11-14, and 20 depend directly or indirectly from claim 1, incorporate the limitations of the base claim, and are thus not anticipated for at least the reasons described above.

Applicant further notes that *Yabe* is silent with respect to "a switch circuit for connecting the first power source and the second power source whose capacity is larger than a capacity of the first source, wherein the switch circuit is

in an off state during a halted state of the clock circuit," as recited in claim 1. Accordingly, claim 1 is allowable for at least this additional reason.

Rejection of Claims 1, 2, 12, 13, and 20 under 35 U.S.C. § 102(b) as being anticipated by *Inoue*:

Applicant traverses the rejection of claims 1, 2, 12, 13, and 20 under 35 U.S.C. § 102(b) as being anticipated by *Inoue*.

Inoue does not disclose each and every element of the rejected claims. For example, *Inoue* does not disclose at least a "a control circuit for, in response to the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit, controlling the switch circuit to turn on in order to connect the first power source and the second power source so that the first power source is charged by the second power source, thereby operating the clock circuit," as recited in amended claim 1.

The Office asserts that the voltage detecting means 4 of *Inoue* corresponds to the claimed "power source input detecting circuit," and that the condenser C1 of *Inoue* corresponds to the claimed "second power source." (FOA at 4.) However, this is not correct. *Inoue* merely teaches that its voltage detecting means 4 detects the voltage of a plurality of condensers. *Inoue* provides no teaching of a "power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit," as recited in claim 1.

Similar to its position discussed above with respect to *Yabe*, the Office also appears to contend that because voltage detecting means 4 of *Inoue*

"detect[s] the input of the second power source at all times" (FOA at 6), *Inoue* necessarily discloses "detecting the insertion of the second power source during a halted state of the clock circuit," as amended in claim 1. However, even if this contention were correct, which Applicant does not concede, *Inoue* still fails to teach or suggest "a control circuit for, in response to the power source input detecting circuit detecting the insertion of the second power source during a halted state of the clock circuit, controlling the switch circuit to turn on in order to connect the first power source and the second power source so that the first power source is charged by the second power source, thereby operating the clock circuit," as recited in amended claim 1.

For at least these reasons, *Inoue* does not disclose each and every element recited in claim 1 as is required to uphold a rejection under 35 U.S.C. § 102(b). *Inoue* thus does not anticipate claim 1. Claims 2, 12, 13, and 20 depend directly or indirectly from claim 1, incorporate the limitations of the base claim, and are thus not anticipated for at least the reasons described above.

Conclusion

In view of the foregoing remarks, Applicant respectfully requests reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully Submitted

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Dated: November 30, 2009

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